REMARKS

Claims 1-21 are pending in the application. The specification and claims 1, 8, 10, 11, 16, 18, 20, and 21 are amended to clarify the subject matter recited therein and/or to correct typographic errors. No new matter is added by these amendments.

The specification is objected based on an informality, and is consequently amended. Therefore, it is respectfully requested that the objection to the specification be withdrawn.

Claims 1 and 11 are objected to based on informalities. Claims 1 and 11 are amended as suggested by the Examiner, and therefore it is respectfully requested that the objections to these claims be withdrawn.

Applicant notes with appreciation that the Examiner acknowledges that claims 5-9 and 15-19 are directed to allowable subject matter.

Claim 21 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 21 is amended to clarify that the term "said program element" refers to "said plurality of program elements" referred to in claim 11, from which claim 21 depends. Therefore it is respectfully requested that the rejection of claim 21 be withdrawn.

Claims 1-4, 10-14, 20, and 21 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,163,488 to Tanizaka et al. (hereinafter Tanizaka). Applicant respectfully traverses.

Claim 1 is directed to a redundancy control circuit that includes, *inter alia*, a plurality of program elements in which a defect address indicating a position of a defect is programmed by a dielectric breakdown due to applying of a voltage. Claim 1 further includes a voltage control section which applies said voltage to part of a plurality of targeted program elements simultaneously. In claim 1, the plurality of targeted program elements are part of the plurality of program elements to be dielectrically broken down correspondingly to said defect address.

Applicant respectfully submits that Tanizaka does not disclose, or even suggest, a plurality of program elements in which a defect address indicating a position of a defect is programmed by a dielectric breakdown due to applying of a voltage. The Office Action cites element 1 of Tanizaka as disclosing this feature. However, both of figures 1 and 4 of

Tanizaka show only a single element 1. Furthermore, there is no discussion in the section cited in the Office Action of more than one element 1. Therefore, even if element 1 of Tanizaka did anticipate a program element, which is respectfully not conceded, Tanizaka does not disclose, or even suggest, a ***plurality of program elements,*** as recited in claim 1. Since the reference does not identically disclose or suggest all of the features of claim 1, the reference does not anticipate claim 1.

Additionally, Tanizaka does not disclose or suggest a voltage control section which applies said voltage to part of a plurality of targeted program elements simultaneously. The Office Action cites a section of Tanizaka that apparently discusses antifuse 61 being blown and serving as a resistant element. However, since Tanizaka does not disclose more than one element 1, as discussed above, Tanizaka cannot disclose a ***simultaneous*** application of voltage to multiple elements. Therefore, for this additional reason claim 1 is allowable.

Furthermore, Tanizaka does not disclose, or even suggest, the feature of a plurality of targeted program elements being part of a plurality of program elements to be dielectrically broken down correspondingly to a defect address. The Office Action fails to cite a particular section of Tanizaka that discloses this feature, and only cites column 5, lines 11-21, in rejecting the claim. Applicant respectfully submits that the cited section does not disclose this feature and respectfully requests a citation to Tanizaka disclosing this feature, or alternatively, that the rejection be withdrawn.

Claims 2-10 depend from claim 1 and are therefore allowable for at least the same reasons as claim 1 is allowable.

Claim 11 is directed to a semiconductor memory that includes, *inter alia*, a plurality of program elements in which a defect address indicating a position of a defect programmed by a dielectric breakdown due to applying of a voltage. Claim 11 further includes a voltage control section which applies said voltage to part of a plurality of targeted program elements simultaneously. In claim 11, the plurality of targeted program elements is part of said plurality of program elements to be dielectrically broken down correspondingly to said defect address.

As discussed above in regard to claim 1, which includes similar features, Tanizaka does not disclose, or even suggest, the features of: a plurality of program

elements in which a defect address indicating a position of a defect is programmed by a dielectric breakdown due to applying of a voltage; a voltage control section which applies said voltage to part of a plurality of targeted program elements simultaneously; and the plurality of targeted program elements is part of said plurality of program elements to be dielectrically broken down correspondingly to said defect address. Applicant respectfully submits the argument presented above in regard to claim 1 in favor of the allowability of claim 11, and requests that the rejection of the claim be withdrawn.

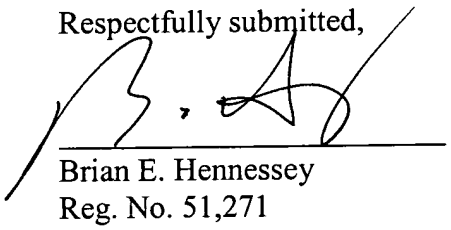
Claims 12-21 depend from claim 11 and are therefore allowable for at least the same reasons as claim 11 is allowable.

CONCLUSION

In view of the above remarks, it is believed that claims 1-21 are in condition for allowance, which action is respectfully solicited. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



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